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APPLICANT
FUJISAKI et al

FILING DATE
July 23, 2003

GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
	4 5 4 4 4 1 7	10/85	Clarke			
	4 6 1 8 3 9 6	10/86	Shimoda			
	3 8 3 3 3 4 2	9/74	Holliday			
	3 4 4 6 6 0 3	5/69	Loiacono			
	3 0 3 3 6 6 0	5/62	Okkerse			
	4 2 9 9 6 5 0	11/81	Bonner			
	2 9 0 8 0 0 4	10/59	Levinson			
	4 5 3 9 0 6 7	9/85	Washizuka			
	4 5 8 6 9 7 9	5/86	Katsumata			
	4 6 3 7 8 5 4	1/87	Fukuda			
	4 6 4 5 5 6 0	2/87	Matsumoto			

FOREIGN PATENT DOCUMENTS

DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION
					YES NO
55 1 1 3 6 9 9	9/80	Japan			X

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

Ghandhi, S. VLSI Fabrication Principles, John Wiley, 1983 pp 86-90, 98-100
Sze, S., Physics of Semiconductor Devices, John Wiley, 1981, p 33
IEEE Transactions on Electron Devices, vo. ED-31, No. 8, Aug. 1984, pp 1057, para 4 5; New York, US; S. Miyazawa

EXAMINER

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